Contributed paper

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MCT sensor readout devices with charge current injection and preliminary signal treatment. Testing procedure

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Silicon read-out devices with input direct injection and buffered direct injection circuits and charge coupled devices (CCD) multiplexers to be used with n^+–p photovoltaic (PV) multielement arrays were designed, manufactured, and tested at T = 77-300 K. Into these readout devices testing switches were incorporated which attach the sources of direct injection transistors to the common load resistors to imitate the output signal of mercury cadmium telluride (MCT) photodiodes. The silicon readout devices for 2×4×128(144) arrays [two sets of 128 or 144 lines (channels) with four pixels in row] in which time delay and integration (TDI) is performed with skimming and partitioning functions, were manufactured by n-channel MOS technology with buried channel CCD register. The designed CCD readout devices are driven with four- or two-phase clock pulses. The amount of charge, which can be stored in the readout device, depends on the mode used. Without skimming and partitioning modes it is 2.4 pC per channel at an output signal of about 5 V. With partitioning mode included it is about 6.4 pC, and it is about 10.0 pC with skimming and partitioning modes switched on. Different operating modes depending on the application purposes can be selected taking into account programmable integration time, possible operation with and without TDI function, availability of skimming level and partitioning factor, etc.

Keywords: HgCdTe photodiodes, CCD read-out devices, buried channel, skimming, partitioning, TDI.

1. Introduction

High performance IR imaging systems for, e.g., surveillance and reconnaissance applications, currently include focal plane arrays (FPAs) with multielement scanning linear (or multilinear) and staring two-dimensional matrix of PV detectors cooled down to cryogenic temperatures with a signal processor in the focal plane. The FPA technologies mainly include two major technologies, hybrid, and monolithic one. The concept of the IR FPA hybrid technology is widespread as permits to optimise separately parameters of detector array with a large number of sensitive elements and typically silicon readout device coupled with detector array [1]. The major hybrid technology uses mercury-cadmium-telluride (MCT) PV detector chips and silicon CCD or CMOS chips [1,2] for readout and multiplexing the sensed charge from the detectors; there are a lot of various designs of interface but really it is a source coupling or a gate coupling [3-5].

The performance requirements for IR FPAs significantly vary with respect to wavelength region, background photon flux, operating temperature, dynamic range, noise, readout rate, power dissipation, detector bias, and some other parameters. IR FPAs are mainly clustered in the atmospheric window wavelengths 1–2.5, 3–5, 8–12 μm and in dependence on the wavelength region applications are aimed at T ≈ 250–300, 77–150, 20–90 K operating temperatures, respectively. The performance of the IR FPAs is mainly determined by the charge stored in the input stage of the signal processor.

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The primary function of a read-out device for IR arrays is to provide an IR detector charge to voltage conversion, integration the electrons generated in a photodetector, permission to perform some preliminary treatment of the signals, e.g., skimming, partitioning, amplification and time multiplexing of signals from the detectors in the array [4], to smaller number of outputs from, as a rule, cold zone. For array, used in scanning mode, TDI function should be included to improve its performance. And the main requirement for IR readout electronics is as follows: it should not limit the performance of the detector in the array. Present IR FPA for 8–12 μm spectral region due to large ≥300 K background flux are faced the problem of large charge integration implying a large charge integration capacitor. Thus, the background signal suppression should be used and this function must be performed in a short time compared with a total integration time.

The aim of this paper is to present some features of some readout integrated circuits (ROICs) to be hybridised with MCT scanning arrays operating, e.g., under noticeable background flux conditions, and thus, with included current skimming and partitioning functions. Here are discussed some properties of CCD signal processors for read-out and multiplexing of hybrid FPA which uses backside illuminated intrinsic PV detectors source coupled with these processors.

The topic of this paper is connected with IR readout electronics, which is of independent interest. For preliminary selection of the silicon read-out devices there was designed a construction of testing circuits incorporated into the read-out devices to test and optimise their parameters before the hybridisation process.

2. Requirements for CCD and circuit approaches

There are several possible main types of architecture and circuit approaches for read-out electronics (see, e.g., Refs. 1,4–6). Here there were chosen CCD--type circuits because of the possibility to realise the lower level of noise, compared to such kind of CMOS-type circuits in spite of the need to use the specific production line for their manufacturing. Though the integration possibilities are less than those of CMOC lines, the design rules 1.5 μm used were enough to get all the functions needed for production of the readout devices with a pitch of approximately 45 μm in PV arrays for which these ROICs were designed and manufactured. Another reason for the CCD approach is connected with the best possible solution for improved performance when TDI concept is used and more flexibility of operating conditions due to higher number of external biases and clocks required (see, e.g., Ref. 2).

For manufacturing of the CCD readout devices a 1.5 μm design rules standard silicon process was used here with two polysilicon gate levels and one metal level, which combines n-channel MOS transistors on the same wafer. The four-inch boron-doped p-type <100> Si wafers with resistivity of 10-20 Ω cm were taken for the process. The large scale integration (LSI) circuit under the consideration consists of MOS transistors with gates from the first and second polysilicon level and CCD cells with buried and semi-buried channels. The direct injection transistors are designed as MOS-transistors with induced channel (the width-to-length ratio $W/L \geq 6$) with first polysilicon level gates. The under-gate dielectric is a thermally grown SiO_2 layer with the thickness of about 500 Å and threshold voltage of approximately 0.3 V.

There are a lot of approaches concerning the problems of IR FPAs and ROICs (see, e.g., Ref. 1, 4 and 5). One of the principal problems limiting the performance of IR FPA deals with limited readout circuit charge handling capacity. To extend the application range of IR imagers to higher background fluxes, higher FPA operating temperatures, higher cut-off wavelengths (λ_{co}) the ROIC should suppresses large useless currents (dark or background) compared to scene photon currents. This situation limits sensitivity and thermal resolution and imposes large constraints on the detector ROICs in terms of dynamic range requirements.

To achieve the suppression of the useless currents prior to CCD multiplexing, several solutions are possible [7–9]. Among them there are: reduction of the incoming photon flux by narrowing spectral band and field of view (FOW) of the detector; reduction of integration time (at a price of a lower signal-to-noise ratio); oversampling (multiple detector signal read out during one sampling); design of various circuits (subframe readout, DC level subtraction, antiblooming, charge partitioning, charge skimming, in-pixel current memory cell, which enables PV direct current suppression [9]), etc. Here, among the available solutions to achieve background suppression in CCD ROICs the classical charge skimming and partitioning functions were chosen, when only a part of charge, according to the background, is subtracted from the integrated charge packet or a fraction of the integrated charge is transferred to CCD, respectively.

In spite of the fact that one can meet some problems with transfer coefficient reducing with lowering the temperature in buried channel CCD (BCCD), because of trapping the electrons in the shallow phosphorous donor level of the CCD buried channel [10,11], this approach was chosen due to superior characteristics of such devices over surface channel CCDs [10,12] (higher transfer efficiency, lower noise, and higher speed operation).

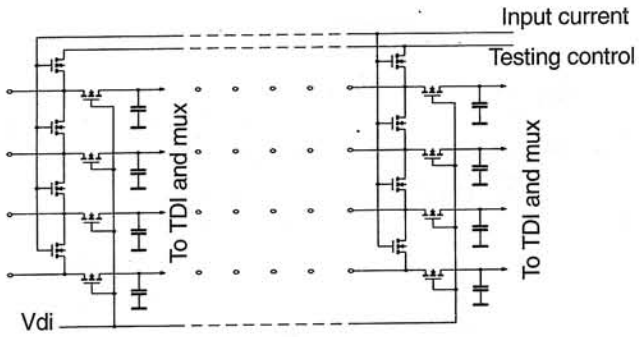


Fig. 1. Testing circuit of the TDI read-out device.

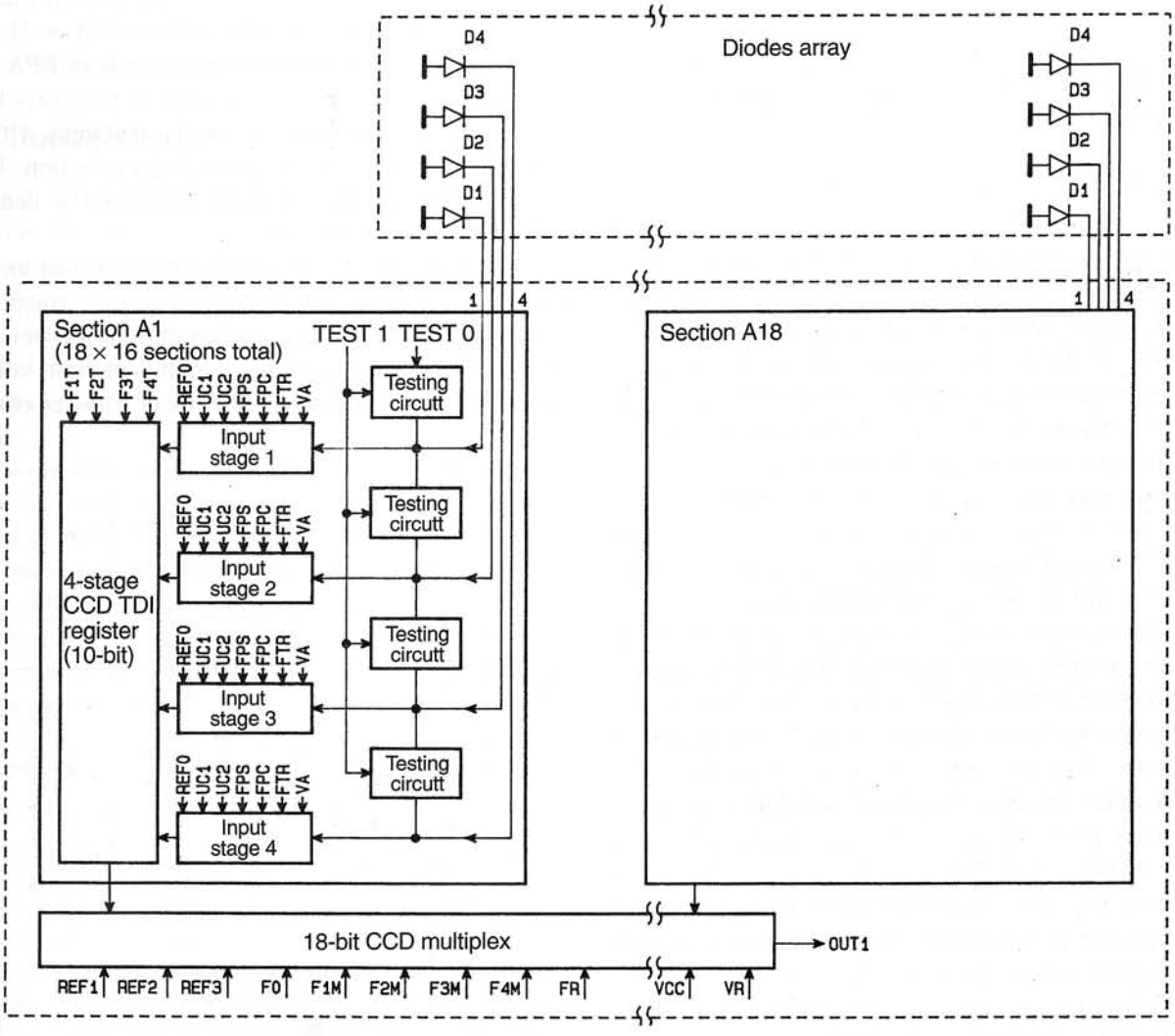


Fig. 2(a). A block diagram of the readout of the format 2×4×144 with testing circuits incorporated. Here REF0 is the bias voltage of the direct injection transistor; UC1 and UC2 are the bias voltages of the storage transistors; FPS is the control voltage of the key which is connecting the storage capacitors C1 and C2; FPC is the control voltage of the key of antiblooming circuit; FTR is the control voltage of the key of the charge transfer from the storage capacity C2 to TDI register; VA is the bias voltage of the antiblooming circuit; TEST0 is the bias voltage of the testing transistors sources; TEST1 is the bias voltage of the testing transistors gates; F1T, F2T, F3T, and F4T are time voltages of CCD TDI registers, F1M, F2M, F3M, and F4M are time voltages of CCD multiplexer; REF1 and REF2 are the bias voltages of the input charge device of the CCD multiplexer; REF3 is the bias voltage of the last electrode of CCD multiplexer; F0 is the control voltage of the charge transfer keys from TDI register to multiplexer register; FR is the control voltage of the precharge key of the CCD multiplexer output device; VR is the bias voltage of the CCD multiplexer output device; VCC is the feeding voltage of the CCD multiplexer output stage.

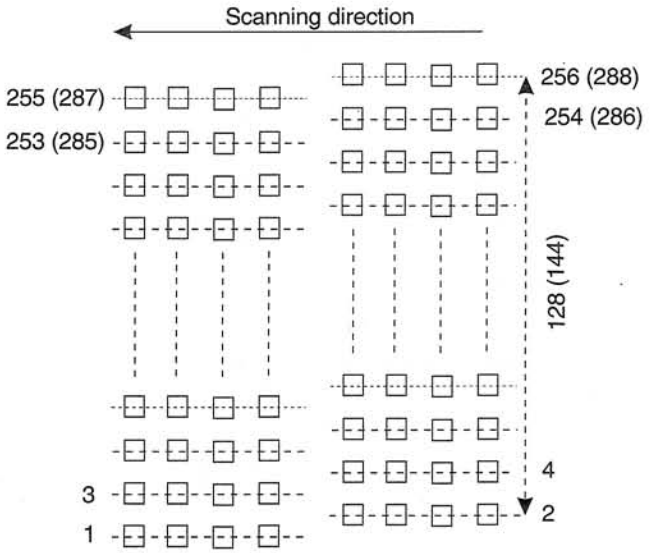


Fig. 2(b). Schematic diagram of the photodiodes displacement.

To test the read-out devices without connecting to photodetectors one needs to provide the availability circuits testing at every input of the read-out device, because, as a rule, it is rather difficult to contact a large number of input bonding pads (with dimensions about 10×10 μm or 15×15 μm for In bumps) with the help of serial probe heads. The testing circuits should be simple and take a small square, not supply an additional noise when operating in hybrid arrays, and should not need a large number of additional electrical buses and additional control impulses.

These demands seem to satisfy the circuits of incorporated into the readout 2×4×128(144) TDI devices for PV diode arrays [see Fig. 1 and Fig. 2(a)]. In Fig. 2(a) it is shown the block diagram of the 2×4×144 device, and in Fig. 2(b) it is shown the topology of PV detectors to which the input transistors of ROICs should be connected by In bump technology. In the array size 2×4×128(144), digit 2 denotes two sets of 128 or 144 lines [see Fig. 2(b)] with four pixels in row in which TDI function is performed. These lines are shifted by half of pitch with respect to each other.

The testing transistors are connected to TDI inputs (see Fig. 1). Applying the opening potential to the gates of testing transistors (the "testing control") it is possible to imitate the flow of photocurrent to the input of direct injection transistor, when putting at the "input current" the total current, which is equal to photocurrent. Here, at temperatures T = 77–300 K some characteristics of the read-out devices pointed out were investigated.

The designed read-out circuits include: one input stage for each PV MCT detector, one four- or two-phase CCD TDI multiplexer with 10 stages for a set of four pixels in row corresponding to one channel, one four- or two-phase CCD multiplexer for eighteen or sixteen channels connected to one output, and two groups of eight outputs of odd and even channels, respectively.

2.1. Unit cell electronics

Unit cell electronics is the most important part of the readout device and should provide perfect bias control, high linearity, and low noise performance. There exist several possible solutions of it [1,4,5]. Among them, to satisfy the requirements of FPA with PV HgCdTe detectors for operation at relatively large backgrounds, there were chosen the unit cells with direct injection (DI) and buffered direct injection (BDI) [13] to improve the coupling between PV detector and CCD signal processor.

Characteristics of direct injection transistor are important for read-out device performance. Extraction of diode current takes place in conditions of potential variation at storage capacity, which is at drain voltage variations. For maintenance of linear transfer charac-

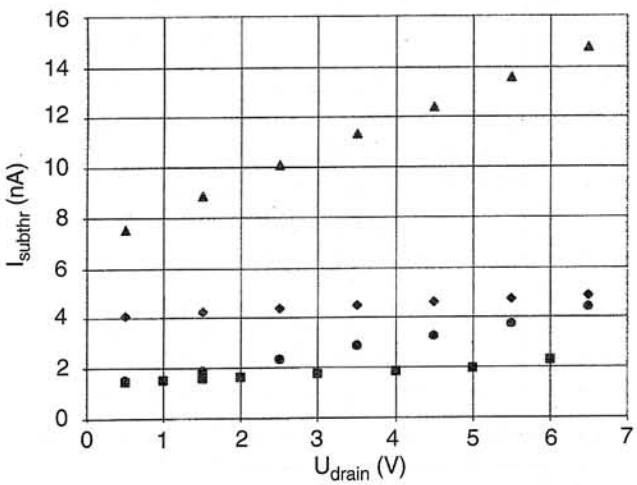


Fig. 3. The dependence of transistor subthreshold current I_{subthr} on the value of drain voltage U_{drain}. ● – channel length 5 μm, T = 293 K; ■ – channel length 6 μm, T = 293 K; ▲ – channel length 5 μm, T = 77 K; ◆ – channel length 6 μm, T = 77 K.

teristics of the read-out devices the drain current of direct injection transistor should not depend on drain voltage. For long channels (L = 15.5 μm) it is a well-known fact [14]. However, for the transistors with such long channels it is difficult to provide the necessary W/L relationship. Subthreshold transistor characteristics investigations with different channel

lengths have shown that in the range of U_{drain} from 0–7 V there are no substantial influence of drain voltages on subthreshold current dependencies at drain length $L \geq 6$ μm. To exclude the dependence of drain current on the drain voltage (see Fig. 3) in the regime of subthreshold currents, the channel length of these transistors were taken $L = 8$ μm.

Transistors, serving as testing circuits of the read-out device, were designed as MOS-transistors with the second polysilicon level gates with the thickness of under-gate SiO_2 d = 1000 Å. The threshold voltage of these transistors, taking into account the boron doping of channels region, is ≈ 3.5 V. The accumulation capacitors are designed as gates from first level polysilicon.

2.2. Buried channel multiplexers

CCD buried channel approach [10,11] was chosen because of superior characteristics of such devices over surface channel CCDs [10,12,15] (higher transfer efficiency, lower noise, and higher speed operation). Though a charge storage capacity in surface channel devices is higher and useful operation is maintained down to lower temperatures compared to BCCD [16].

Taking this into account, here the multiplexers were designed according to CCD technology with buried channel. To simplify the external control circuits, the CCD cell with asymmetric potential well is used (with two or one and a half phase control). The storage charge region is created by phosphorus ion implantation (D = 0.16 μC, E = 100 keV) into the under the gate region from polysilicon first level. To fabricate the barrier regions under the gates from polysilicon second level there is used second boron implantation (D = 0.12 μC, E = 60 keV), which compensates the part of introduced phosphorus. The resulting depth of potential well for information charge storage is about 5 V, and multiplexer charge capacity Q is about Q ≈ 2.4 pC.

Study of the temperature dependencies of CCD transfer inefficiency has shown its noticeable increase with temperature decrease in agreement with known data (see, e.g., Refs. 10, 11 and 15). As an example of the circuits with two-phase and four-phase driven clock pulses, manufactured from the same Si wafers, the transfer inefficiency characteristics in dependence on temperature are shown in Fig. 4(a). It is clearly seen the same exponential temperature dependence for two types of circuits, which is due to the influence of the freeze-out effect.

Transfer inefficiency was determined by measurements of losses in leading impulse of string pulses. The experiments are made at effective transfer time of 0.125 μs with rise and fall time of 60 ns. At rise and fall time shortening one can observe displacement of the beginning of transfer inefficiency coefficient increase at higher temperatures. The use of longer rise and fall time is limited by the necessity to use CCD ROICs at clocking frequencies not less than 2 MHz. It was shown that in the range of clock frequency 0.5–2.0 MHz the charge transfer inefficiency only slightly depends on it, but noticeably depends on the signal charge value [see Fig. 4(b)].

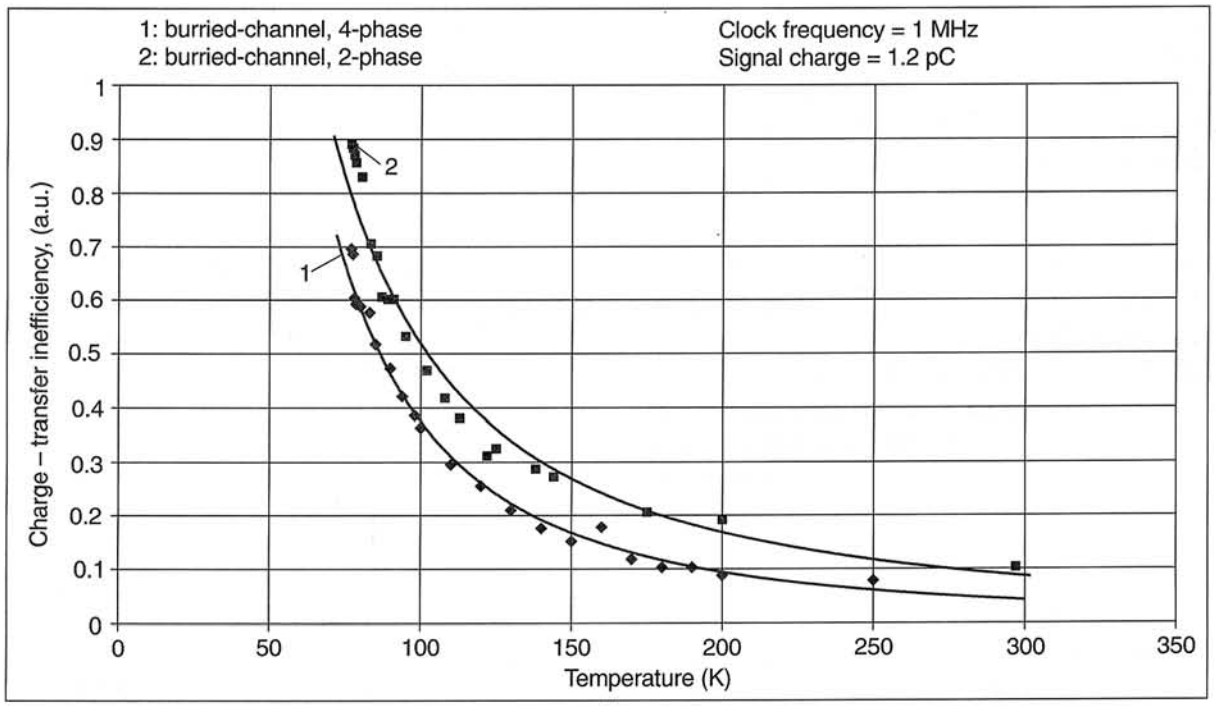
In Fig. 4(a) one can see transfer efficiency degradation at low temperature region which makes the charge transfer process worse to some degree of these ROICs, which are driven by four- or two-phase clock pulses. Because of almost twice smaller number of transfer stages (there are 36 transfer stages in ROICs, driven by two-phase clock pulses, and 64 transfer stages in ROICs, driven by four-phase clock pulses), the transfer efficiency degradation for the whole circuit is less for CCD devices driven by two-phase clock pulses.

Comparison of CCD ROICs driven by two-phase and four-phase clock pulses have shown that in two-phase system the transfer efficiency is higher at low temperatures because of less number of transfer stages, though the manufacture technological procedure is simpler in the last case. Two-phase CCD ROICs are simpler for using and they have smaller number of connections needed for cold zone, which lowers the heat load. The possibility to get larger storage capacity in the case of four-phase devices compared to two-phase circuits, is not a restriction in this case as in read-out devices for IR PV HgCdTe detectors, as here is the possibility to have large storage capacities due to the constructional peculiarities of these devices, and receiving of large square electrodes is not a restriction.

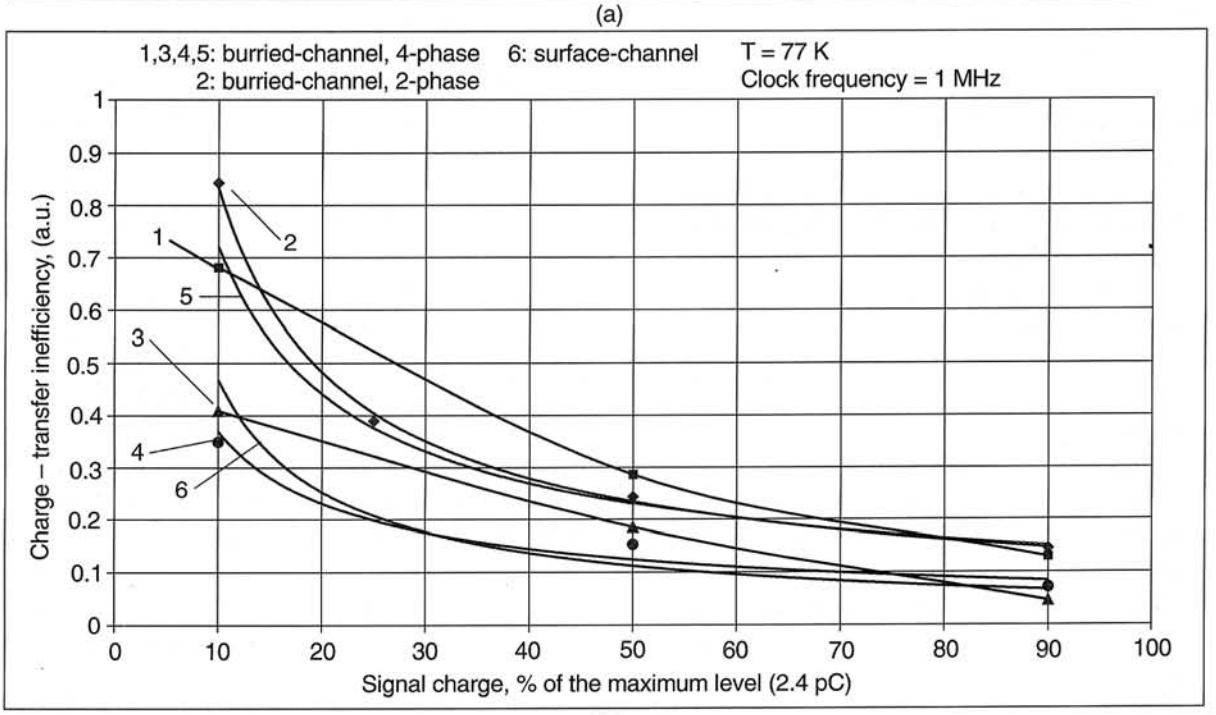
Despite the fact that for four-phase CCD ROIC there exists the possibility to organise the reverse movement of the charge flow, here it is not very important because of TDI small number of stages and, as a rule, the presence of antiblooming circuit for each photodiodes and skimming and partitioning modes. Measuring the parameters of designed devices (18-bit register-multiplexer) did not show large difference in dynamical range and linearity.

2.3. TDI function

Displacement register of TDI with four inputs of information charge is also designed as CCD cells with asymmetrical potential well. To increase its charge ca-



(a)



(b)

Fig. 4: (a) Temperature dependence of relative transfer inefficiency dependence in BCCD with two-phase and four-phase driven clock pulses (a). Channel depth d = 2.5 μm, surface concentration $N_d = 1\times10^{12}$ cm^{-2}, substrate free carrier concentration $N_a = 1\times10^{15}$ cm^{-3}. For first level polysilicon electrode channel width W = 130 μm, channel length L = 14 μm, and for second level polysilicon electrode channel width W = 130 μm, channel length L = 7 μm. Gate length is equal to 17 μm. Clock frequency f = 1 MHz. Maximum signal charge level is 2.4 pC.
(b) Transfer inefficiency dependence in BCCD with two-phase and four-phase driven clock pulses in dependence of signal charge level at temperature T = 77 K. Maximum signal charge level is 2.4 pC.

pacity the technology of "semi-buried" channel is used, which differs compared to buried channel with the potential at the barrier gate. In the case of "semi-buried" channel charge capacity regions, under first polysilicon level, are manufactured by phosphorus ion implantation at the same time with manufacturing the capacity

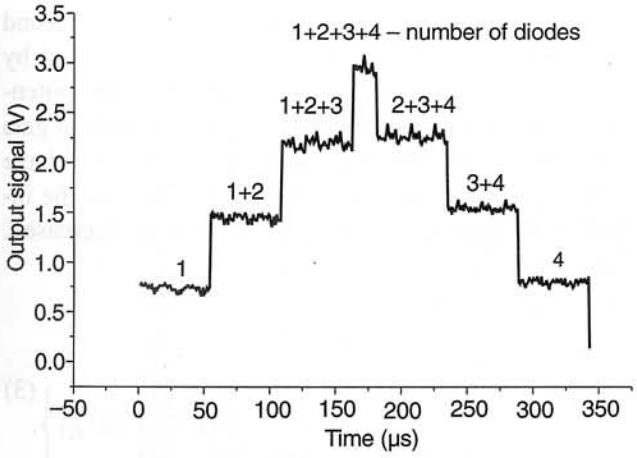


Fig. 5. An example of CCD cell operation with four stages TDI function.

regions in multiplexer, and in barrier region there is executed the addition boron implantation with D = 0.05 μC, E = 60 keV, that increases the depth of the potential well to ≈ 8 V. The charge capacity of the TDI register output bit is about 2.4 pC per channel at an output signal of about 5 V. With partitioning mode included it is about 6.4 pC, and it is about 10.0 pC with skimming and partitioning modes switched on both for four- and two phases clock pulses CCD ROICs. The example of CCD cell operation with four stage TDI function is shown in Fig. 5 for ROIC driven with four phases clock pulses. Here there are shown the signal amplitudes from one, from the sum of two, three, and four diodes, respectively.

2.4. Charge skimming and partitioning modes

When charge skimming mode is applied, a constant portion of charge, according to the background flux, is subtracted from the integrated charge packet. In the case of using partitioning mode only a fraction of the integrated charge is transferred to the CCD, the partitioning ratios can be changed according to the user's requirements.

High intensity of background radiation and long integration time (particularly in the case of PV detector and low R_oA product value) can lead to the overflow of accumulation capacity. In this case it is necessary to use the skimming mode or partitioning mode, or skimming and partitioning modes simultaneously according to user's requirements. To maintain this feature of readout device here several elements are added into the input circuits. There are skimming/partitioning gate G1, CCD transfer control gate G2, capacity C2 (Fig. 6), skimming/antiblooming transistor for extraction of the charge excess.

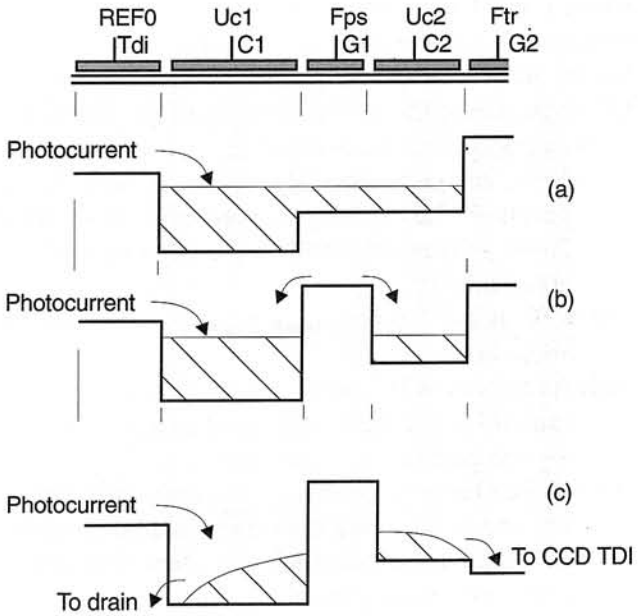


Fig. 6. Schematic potential and charge distribution at skimming/partition mode.

2.5. Partitioning mode

In this mode the electrodes C1 and C2 are connected together and constant value direct voltage is applied to them. The pulse voltage is applied to the partitioning gate G1, the CCD transfer control gate G2 and gate of extraction transistor. The integration time period T_{F1}, the accumulation of signal charge takes place into the capacitors C1 and C2. To partitioning the electrode G1 during the integration processes the high potential is applied which provides free charge flow from one capacitor to another and also equalising these capacitance potentials. Then, the channel between them is switched off and full signal charge is divided between two capacities, proportionally to their values (both information and noise charges). C2 capacity charge is an information charge and C1 capacity charge is removed into reset transistor drain. In this mode an extra noise charge is caused with uncertain set in potential (often referred as kTC noise) and direct voltage noise of checking electrodes.

Summary noise can be expressed as

$$\Delta Q_\Sigma^2 = \frac{1}{m^2} \left\{ \Delta Q_0^2 + kTC + C^2(\Delta U_1^2 + \Delta U_2^2) + kTC_{G1} \right\}, \quad (1)$$

where $C = C1 + C_2$, $m = C_2/(C_1 + C_2)$ is the divide coefficient, ΔQ_0 is the input noise charge, ΔU_1 and ΔU_2 are the noise level of the potential electrodes G1 and G2 respectively, C_{G1} is the capacity of the gate G1.

Numerical considerations of Eq. (1) show that:

(i) Noise charge of input signal at background temperature 120°C and integration time over 20-40 μs is about 3000-4000 e [first term of expression (1)],

(ii) kTC noise [second term of expression (1)] is about 60 e,

(iii) Additional kTC noise (third term), which is caused by uncertain of refused charge being under the gate G1, is about several e,

(iv) Noise charge is caused by the gate noise potential and is not more than one hundred electrons at 100 μV noise potential, and about thousand of e at 1 mV noise potential [forth and fifth terms of Eq. (1)].

Total deterioration of signal-to-noise ratio (and naturally deterioration in minimum noise equivalent difference temperature (NEΔT) is not more than 1–2% at well stabilised direct voltage (noise potential lower than 100 μV) and about 25–30% at usually used stabilisation level (noise potential about 1 mV).

2.6. Skimming mode

In this mode constant voltage is applied to skimming the gate G1. A value of this voltage is lower then voltage applied to the gate C1 and C2, therefore it is potential barrier between the charge capacities C1 and C2. A constant value of input charge is subtracted from total input charge and it is refused at the pre-charge time into skimming transistor drain. The value of a fixed input charge is determined by dimensions of capacitor C1 and different potentials under the gates C1 and G1. Part of the input charge that is flowing across a potential barrier is a signal charge and it is transferred into CCD TDI. Of course, total input noise charge is transferred into CCD. As in partition mode an additional noise is caused by kTC noise (uncertain set in potential under the electrodes C1 and G1) and direct voltage noise of these electrodes.

In this case the total noise charge that is transferring in CCD is

$$\Delta Q_\Sigma^2 = \Delta Q_0^2 + C_1^2 \left\{ kT\left(\frac{1}{C_1} + \frac{1}{C_{G_1}}\right) + \Delta U_1^2 + \Delta U_{G_1}^2 \right\}, \quad (2)$$

where ΔU_{G1} is the potential electrode G_1 noise.

In this circuit, kTC noise is about 120 e [second term of Eq. (2)]. Noise charge, which is caused by noise potential, is about 230 e at 100 μV noise potential (third and forth terms). If the gate G1 and the gate capacitor C2 are electrically connected, one will have a modification of skimming mode. In this case the influence of gate G1 to additional noise is decreased. Total noise is equal:

$$\Delta Q_\Sigma^2 = \Delta Q_0^2 + C_1 \left\{ kT\left(\frac{1}{C_1} + \frac{1}{C_2 + C_{G1}}\right) + \Delta U_1^2 + \Delta U_{G1}^2 \right\}. \quad (3)$$

2.7. Skimming plus partitioning mode

If one applies, to the electrode C2, the direct potential lower than to the electrode C1, the amplitude Ups of the pulse Fps equals the direct potential C2, it is possible the part of input charge to be subtracted and other part of charge is divided proportionally to the capacities C1 and C2. The noise processes of skimming plus partitioning mode is similar to only partitioning mode. Because the noise charge is much less compared to charge capacity of C1 and C2 electrodes, the expression for the total noise is similar to Eq. (1).

Numerical consideration of all expressions shows that any mode of total deterioration of signal-to-noise ratio (and thus, deterioration in minimum NEΔT) at the high intensity of background radiation and long integration time is several percent at well stabilised direct voltage (noise potential lower than 100 μV), but at usual stabilisation level (noise potential about 1 mV) deterioration will be about 1.5–2 times higher.

Applying skimming and partitioning modes leads to noise enhancement but allows to expand the dynamic range, e.g., to extend the application range of CCD FPA to higher background temperatures, longer wavelength regions. Different operating modes, depending on the application purposes, can be selected taking into account programmable integration time, possible operation with and without TDI function, availability of skimming level and partitioning factor, etc.

3. Selection of testing mode of the circuit

For identical mode CCD multiplexer performance insurance, the measurements of the parameters were carried out for the same current and frequency intervals at room and liquid nitrogen temperatures.

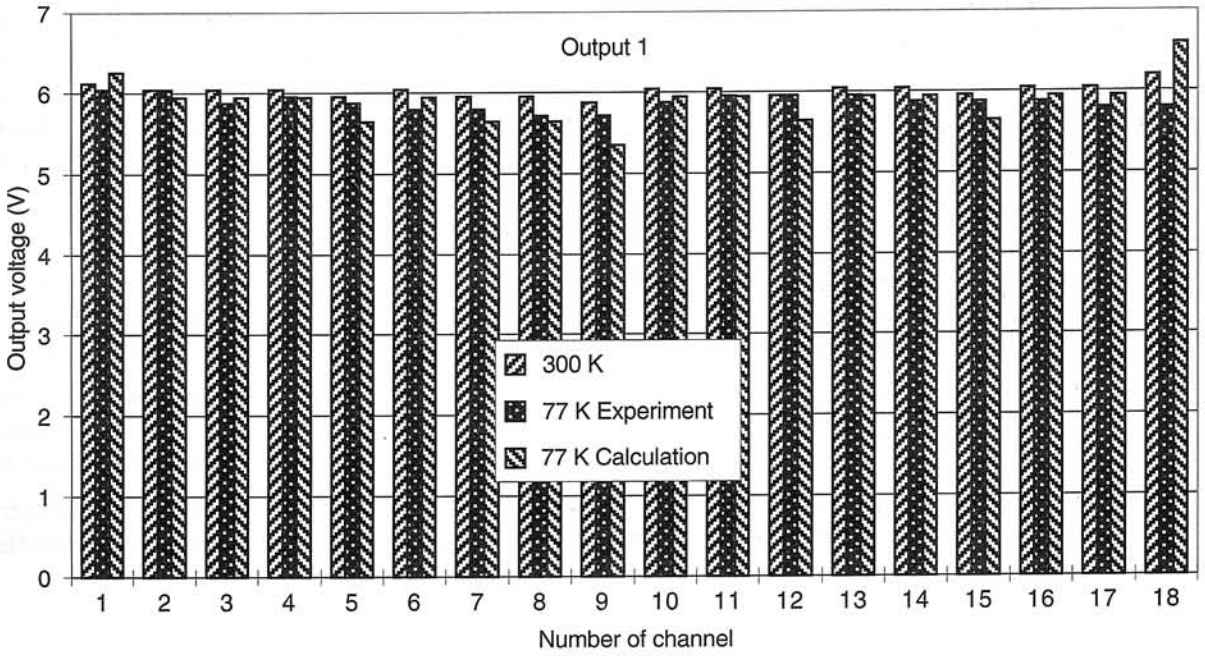


Fig. 7. Dependencies of multiplexer output voltages on channel number in typical sample of the read-out device for two outputs at T = 300 K, and T = 77 K (experimental and calculated data).

In the underthreshold mode, the transistor current i depends on ratio of the potentials at its electrodes to thermal potential

$$i = i_0 \exp \frac{q(U_G - U_S - U_T)}{nkT}, \tag{4}$$

where [17]

$$i_0 = \mu \frac{W}{L} C_{ox} (n-1) \left(\frac{kT}{q}\right)^2. \tag{5}$$

Here q is the electron charge, k is the Boltzmann constant, T is the temperature, U_G and U_S are the voltages at the transistor gate and source, respectively; U_T is the transistor threshold voltage, n ≈ 2 is the constant, μ is the carrier mobility, W and L are the width and length of the transistor gate, respectively; and C_{ox} is the specific capacity of the gate oxide.

For photocurrent imitation to the "input current", output is attached the resistor R. The injection coefficient η of this circuit is defined by the ordinary expression

$$\eta = \frac{gR}{1+gR}, \tag{6}$$

where g is the steepness of N parallel attached transistors

$$g = \frac{q}{nkT} \sum_{s=1}^{N} i_s \approx \frac{q}{nkT} Ni. \tag{7}$$

Inserting expression (7) in expression (6) and taking into account that $U_S = R \times N \times i_s$ one obtains that for given circuit the injection coefficient is determined by source potential to thermal potential ratio

$$\eta = \frac{qU_s/nkT}{1+qU_s/nkT}. \tag{8}$$

It follows from Eqs. (4) and (8), that during the read-out devices testing procedure one should change the potentials at the electrodes of direct injection transistors proportionally to temperature change, at which the circuit parameters measurements are carried out.

In Fig. 7 there are shown the results of measurements of typical multiplexer output voltages for T = 300 K and T = 77 K. The difference in amplitudes of output voltages is mainly connected with difference in direct transistors threshold voltages in different channels.

For given testing method, the deviation of threshold voltages of direct injection transistor manifests itself stronger than in the case of testing procedure with photodiodes at transistors inputs.

The dependencies of multiplexer output signals on current imitation with testing circuits in different

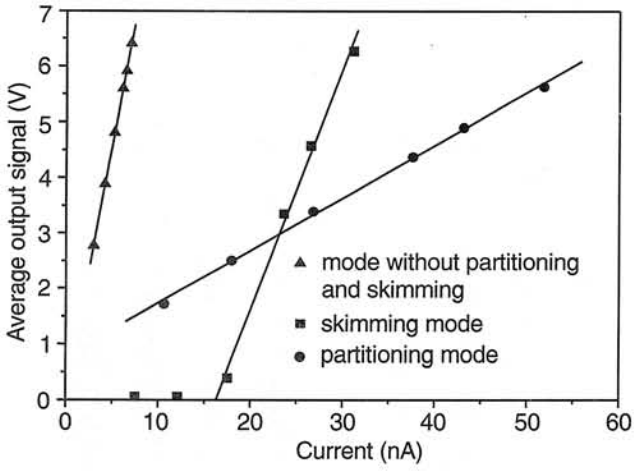


Fig. 8. Typical dependencies of multiplexer output signals on current imitation with testing circuits for one of the read-out device sample.

modes (without and with skimming and partitioning modes) are shown in Fig. 8. Character of dependencies shown is linear within 2% that confirms the influence of drain voltage on the direct injection transistor current.

4. Analysis of the experimental results

Let us assigned the output voltage (of the channel) of the multiplexer, which corresponds to r-input by U_r, and geometrical average value of the output voltage at every output by

$$< U > = \left(\prod_{r=1}^{N} U_r \right)^{1/N} . \tag{9}$$

From Eqs. (4) and (9) it follows

$$\frac{U_r}{< U >} = \frac{i_{0r}}{< i_0 >} \exp\left\{ -\frac{q\Delta U_{Tr}}{nkT} \right\} = \exp\left\{ -\frac{q}{nkT} \left[\Delta U_{Tr} - \frac{nkT}{q} \ln \frac{i_{0r}}{< i_0 >} \right] \right\}, \tag{10}$$

where

$$\Delta U_{Tr} = U_{Tr} - \overline{U}_r = U_{Tr} - \frac{1}{N} \sum_{s=1}^{N} U_{Ts}. \tag{11}$$

Let us transform the second item (in square brackets) of Eq. (10)

$$\ln \frac{i_{0r}}{< i_0 >} = \ln \left(1 + \frac{i_{0r} - < i_0 >}{< i_0 >} \right) = \ln \left(1 + \frac{\Delta i_{0r}}{< i_0 >} \right) \approx \frac{\Delta i_{0r}}{< i_0 >} . \tag{12}$$

From Eq. (5) it follows

$$\frac{\Delta i_{0r}}{< i_0 >} = \frac{\Delta \mu_r}{< \mu >} + \frac{\Delta W_r}{< W >} - \frac{\Delta L_r}{< L >} + \frac{\Delta C_{ox,r}}{< C_{ox} >} = \frac{\Delta \mu_r}{< \mu >} + \frac{\Delta W_r}{< W >} - \frac{\Delta L_r}{< L >} - \frac{\Delta \delta_r}{< \delta >}, \tag{13}$$

where δ is the thickness of the undergate dielectric.

Let us introduce the notion of the effective deviation of the threshold voltage $\Delta U_{T,eff}$

$$\Delta U_{T,eff} = \Delta U_T - \frac{nkT}{q} \frac{\Delta i_0}{< i_0 >}. \tag{14}$$

From Eq. (10) one can obtain

$$\Delta U_{Tr,eff} = -\frac{nkT}{q} \ln \left(\frac{U_r}{< U >} \right). \tag{15}$$

Calculated from amplitudes of multiplexer output voltages of direct injection transistors are shown in Fig. 9. One can see that deviation of the threshold voltage decreases with temperature decrease, which is in correspondence with equation (15). For the chosen testing procedure the deviation of effective threshold voltages can be within the value of ±0.5 mV.

It is important to mention that deviation of the photodiodes bias (which is equal to the source voltage

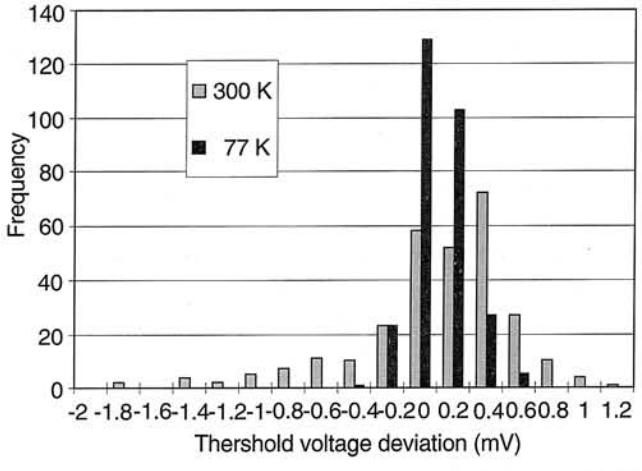


Fig. 9. An example of deviation of direct injection transistor threshold voltages at T = 300 K and T = 77 K.

of the readout transistor U_S) is determined by effective deviation of the readout transistors threshold voltages $U_{T,eff}$ but not by U_T deviations. Really, the transistor current I_{tr} is equal to the sum of the photodiode bias current I_d and the photocurrent I_{ph}

$$I_{tr} = i_0 \exp\left\{\frac{q}{nkT}(U_G - U_T - U_S)\right\} = . \quad (16)$$
$$= I_{ph} + I_d(U_S),$$

where i_0 is the constant which does not depend on U_G, U_T, and U_S.

It follows from Eq. (16) that changes of parameters of the readout transistor (i_0 and U_T) lead to bias voltage changes

$$g\left(\frac{nkT}{q}\frac{\Delta i_0}{i_0} - \Delta U_T - \Delta U_S\right) = \frac{\Delta U_S}{R_d}, \quad (17)$$

where $1/R = dI_d/dU_s$ is the diode dynamical-resistance. In Eq. (17) it is taken into account that transistor steepness in underthreshold regime is $g = qI_{tr}/nkT$. From Eq. (17) it follows

$$\Delta U_S = -\frac{gR_d}{1+gR_d}\Delta U_{T,eff}. \quad (18)$$

Thus, elaborating the construction and technology of the readout devices one should take into account the influence of the different parameters on the effective threshold voltage deviations. Really, if we assume that variables in Eqs. (13) and (14) are independent from each other then for effective threshold voltage dispersion it follows

$$\sigma^2(\Delta U_{T,eff}) = \sigma^2(\Delta U_T) + \left(\frac{nkT}{q}\right)^2 \left[\sigma^2\left(\frac{\Delta\mu}{\mu}\right) + \sigma^2\left(\frac{\Delta L}{L}\right) + \sigma^2\left(\frac{\Delta W}{W}\right) + \sigma^2\left(\frac{\Delta\delta}{\delta}\right)\right]. \quad (19)$$

If, e.g., mean square root deviation of every item in square brackets is equal to 2% then that leads to increase of effective threshold voltage by 4 mV^2 at room temperature. Thus, the presence of testing transistors allows the preliminary selection of the read-out devices with parameters, which ensure lower signal deviation in different channels.

Using the expression (10) one can preview the distribution of the threshold scatter output voltages at other temperature T_1

$$\left.\frac{U_r}{<U>}\right|_{T1} = \left(\left.\frac{U_r}{<U>}\right|_{T}\right)^{\frac{T1}{T}}. \quad (20)$$

The observed experimental data are in good agreement with calculated data according to Eq. (20) (see Fig. 9).

5. Conclusions

Silicon read-out devices with source input circuits and CCD multiplexers to be used with n^+–p PV multielement MCT arrays were designed, manufactured and tested at T = 77–300 K. The silicon ROICs of 2×4×128(144) with TDI function, skimming, and partitioning modes were manufactured by n–channel MOS technology with buried channel CCD registers. The ROICs designed and manufactured give the possibility to store rather large amount of charge. Depending on the mode used it can be changed in wide region. Without skimming and partitioning modes it is 2.4 pC per channel at an output signal of about 5 V. With partitioning mode included it is about 6.4 pC, and it is about 10.0 pC when skimming and partitioning modes both are included.

Comparison of the parameters of CCD ROICs, driven by two-phase and four-phase clock pulses, did not show noticeable differences in transfer inefficiencies at T ≥ 77 K. However, due to almost twice smaller number of transfer stages the transfer efficiency degradation for the whole circuit is less for CCD devices, driven by two-phase clock pulses, compared to those driven by four-phase clock pulses. Comparison of dynamical range and linearity did not show any differences between these ROICs driven by two-phase clock pulses and four-phase clock pulses, respectively.

The results of investigations of the parameters of the ROICs designed have shown the need of high degree of stabilisation of the control voltages in them. Decrease in the stabilisation level from 100 μV to 1 mV leads to increase in the noise level from about 1.3 to 2 times in dependence on the type of the signal charge processing (partitioning, skimming, or partitioning plus skimming).

Including the skimming and partitioning functions gives the possibility, e.g., of the background useless currents suppression to expand the range of the input signals detected, though the noise level is increased. This gives the opportunity to extend the application range of IR imagers to higher background fluxes, higher FPA operating temperatures, higher cut-off wavelengths, etc.

Testing switches incorporated into these ROICs, which attach the sources of direct injection transistors to the common load resistors to imitate the output signal of MCT photodiodes, gave the possibility to apply the testing procedure at room temperature and allowed the preliminary selection of the read-out devices with characteristics which satisfy the performance of the arrays assembling.

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